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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2191	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/003,570	CABILLIC ET AL.	
	Examiner	Art Unit	
	TED T. VO	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to Applicants' amendment filed on 11/30/2009.

Claims 1-15, 18-24 are pending in this application.

Specification

2. It should be noted that this specification has hyperlinks, browser executable code in its reference pages. The specification is objected to.

Response to Arguments

3. This is in response to the argument remarks filed on 11/30/2009.

- In view of the amendment, the rejection of claim 1-8 under 112 second paragraph is withdrawn.

- Regarding to the arguments to the rejections of claims 22-23 and 24. The claims 22-23 direct to a processor and claim 24 directs to two processors. However, none of the elements of the processors is shown. Therefore, it is unable to determine what elements in the claims are claiming for the patent protection. A computer included with one processor or two or more processors is not new. On the other hand, the claims recite merely the program code. The term "comprising" in claims 22-23 shows the claims are a program; however, claims define

"processor". There is no connection between the element processor and the element program code, or at least having essential steps, for showing these two elements are within a single and defined scope. This is indefinite under 35 USC 112 second paragraph since the scope of the claims is ambiguous. Examiner fails to determine the claimed subject matters to define the scope for claims 22-23 and the scope for claim 24 . Applicants submitted theses claims are not indefinite but broad. Applicants submitted case laws. Examiner respectfully disagrees. Not all the broad claims are definite. However, this is not the case for the rejection of these claims. The rejections to claims 22-23 and 24 are maintained for the reason that the scopes of the claims are ambiguous.

See IPXL Holdings, 430 F.3d at 1384. *See also $3 Inc.,* 259 F.3d at 1372 ("When the claims become so ambiguous that one of ordinary skill in the art cannot determine their scope absent speculation, such claims are invalid for indefiniteness.") (citing *In re Steele,* 305 F.2d at 862-63).

- Claims 1-8, 9-10, 11-12, 13-15 and 18-21 are rejected under 35 U.S.C 101:

Claims 11-12, 13-15 and 18-21 recite apparatus claims. Applicants argued the claims meet statutory class, at least it has the claimed preamble provide the weight "for…high level source code and instruction for a target processor" tied with a statutory class.

Examiner respectfully disagrees. The recited claims remain broad that cover non-statutory class. First of all, Examiner recognizes that an apparatus is not only a computer, but it is also any functionality not occurred in the computer like a computer program. The language as agued, "for…high level source code and instruction for a target processor" is merely the

language like "allowing" a computer to do some thing rather then it occurs in a computer. Thus, the apparatus claims cannot be addressed as it is done or within a computer. It covers a computer program per se.

Similarly, Claims 1-8 recite a method for generating program source and claims 9-10 recite a method for creating program source code. However, the language used in preamble "for…high level source code and instruction for a target processor" as mentioned fails to cause the functionality to occur in the computer. The steps in the claims are generic enough in order to take the broadest interpretation. The interpretation is that the methods are mental steps made up by a high level computer program per se. Thus, a method lacks the requirement for producing functionality by the computer; it would fail to produce tangible, concrete, and practical result.

- Regarding to the argument to the claims 1-15, 18-24 rejected under 35 U.S.C. 102(b) by Smith et al..

Applicants are arguments have been considered, but they are not persuasive since the claims are broad, as admiited by Applicants. When the claims are broad, the Examiner take reasonable interpretation for addressing that the reference of Smith meets the broad reciation as mapped. Therefore, in view of the refernce, the broad recitations in the claims read on the reference as provided.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 22-23: The claim recites a processor. Physically, the processor is an apparatus which requires consisting of elements. None of the elements of a processor is shown. It has seen in the claim that its recitation attempts using a method for configuring the processor; its functionality is a process for use. Therefore, it is unclear whether the language of claim 22 and 23 is directed to a processor or a method of using that processor. A reviewing court has determined that a claim directed to a system and a method for using that system is indefinite. *See IPXL Holdings,* 430 F.3d at 1384. *See also \$3 Inc.,* 259 F.3d at 1372 ("When the claims become so ambiguous that one of ordinary skill in the art cannot determine their scope absent speculation, such claims are invalid for indefiniteness.") (citing *In re Steele,* 305 F.2d at 862-63). The interpretation for the claims is they are processor apparatuses.

As per claim 24: The claim recites a system comprising two processors. It shows that the claim merely recite a method for use, configured by upon two program source code modules. The claim is without any elements for structuring a system and/or the two of the processors.

Therefore, it is unclear whether the language of claim 24 is directed to a system of two processors or a method for use. A reviewing court has determined that a claim directed to a system and a method for using that system is indefinite. *See IPXL Holdings,* 430 F.3d at 1384. *See also S3 Inc.,* 259 F.3d at 1372 ("When the claims become so ambiguous that one of ordinary skill in the art cannot determine their scope absent speculation, such claims are invalid for indefiniteness.") (citing *In re Steele,* 305 F.2d at 862-63). The interpretation for the claim is it is a system of two processors.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. The claims 1-8, 9-10, 11-12, 13-15 and 18-21 are rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory subject matter.

As per claims 1-8:

Analysis: Claims 1-8 direct to a method. The scope of the claims recites: "generating program source code for translating high level code into instructions for a target processor". Even the method mentions "target processors", the functionality in the method is not necessary occurs in a computer. The language "target processor" is only an intended purpose.

In the body of the method, none of steps shows it is being done by a computer.

"determining a program code characteristic corresponding to said target processor;

deriving one or more program code modules in accordance with said desired program code characteristic; and

generating program source code for translating high level code into instructions for said target processor from said one or more program code modules".

It appears that with handwriting can form the method. The method appear to be mentally process. Thus it fails to be tangible, concrete, and practical result..

As per claims 9-10: The rejection is applied the same as being analyzed as in the rejection of claims 1-8.

As per claims 11-12:

Analysis: Claims recite "data processing apparatus". As it is known that an apparatus can be a program module. The claims fail to connect to a machine but the claims are only indented for creating program source code. Its apparatus covers a programming per se.

As per claims 13-15, 18-21: The rejection is applied the same as being analyzed as in the rejection of claims 11-12.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-15, 18-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al., "Distributed Programming with Intermediate IDL", June 1999, Ada Letters, Col. XIX, No. 2, pages 90-95.

As per Claim 1: Smith discloses, ***A method for generating program source code for translating high level code into instructions for a target processors, the method comprising: determining a program code characteristic corresponding to said target processor***;

(see Figure 4, JIA; see sec. 3.1, particularly, see sec, 3.1.2, and 3.1.3, the modules are the sources of Ada code and Java code))

deriving one or more program code modules in accordance with said program code characteristic; and

(see abstract (p. 90), see sec. 2, sec 3.2)

generating program source code for translating high level code into instructions for said target processor from said one or more program code modules.

(See Figure 3: IDL Object specifications; see sec. 3, particularly the paragraph in p. 92; see sec. 3.1, particularly, for "modules", see sec, 3.1.2, and 3.1.3)

As per Claim 2: Smith discloses,

A method according to claim 1, for generating program source code for translating high level code (Figure 4-5) ***into instructions for one of a plurality of target processors.***

(see sec. 3, particularly the paragraph in p. 92; see sec. 3.1, particularly, for "modules", see sec, 3.1.2, and 3.1.3)

As per Claim 3: Smith discloses,

A method according to claim 1, comprising forming agglomerated program source code from a plurality of program code modules (See Figures 1,3) ***in accordance with said program code characteristic.***

See Figure 4-5, and see sec. 3.1.1.

As per Claim 4: Smith discloses,

A method according to claim 1, further comprising deriving said program code modules in accordance with a desired functionality for said target processor. See abstract (p. 90: using the IDL, see sec. 2, sec 3.2.

As per Claim 5: Smith discloses,

A method according to claim 2, wherein:

said step of determining comprises determining respective program code characteristics for respective ones of a plurality of target processors;

said step of deriving comprises deriving respective program code modules in accordance with said respective program code characteristics; and

said step of generating comprises generating program source code for translating high level code into instructions for said target processors from said program code modules.

See rationale addressed in the rejection of claim 1.

As per Claim 6: Smith discloses,

A method according to claim 1, wherein said step of deriving comprises selecting one or more pre-defined program code modules in accordance with said program code characteristic from a plurality of available program code modules.

See Figure 4-5, and refer to the use of IDL.

As per Claim 7: Smith discloses,

A method according to claim 1, wherein said program code provides a virtual machine for said target processor. See sec. 2.2 (p. 91).

As per Claim 8: Smith discloses,

A method according to claim 1, wherein said program code comprises elements of a programming language. See Figure 1 or 3.

As per Claims 9, 11: Regarding the limitation recited in claims 9, 11, the functionality of the claims has the same to the functionality recited in Claim 1. See the rationale addressed in the rejection of claim 1 for the rejection to claims 9 and 11.

As per Claims 10, 12: Regarding the limitation recited in claims 10, 12, the functionality of the claims has the same to the functionality recited in Claim 2. See the rationale addressed in the rejection of claim 2 for the rejection to claims 10 and 12.

As per Claim 13: Regarding: *An apparatus, comprising at least one program source code module of a plurality of program source code modules for translating between high level code and instructions for a target processor, said at least one program code module corresponding to a characteristic of said target processor and being selected from said plurality of program source code modules.*

See the rationale addressed in Claim 1.

As per Claim 14: Regarding: *The apparatus of claim 13, further comprising at least one additional program code modules for translating between high level code and instructions for respective ones of at least two target processors.*

See the rationale addressed in Claim 2.

As per Claim 15: Regarding: *The apparatus according to claim 14, wherein said at least two program code modules are selected from a plurality of predefined program code modules.*

See the rationale addressed in Claim 3.

As per Claim 18: Regarding: *The apparatus according to claim 13, wherein said program source code provides a virtual machine for said target processor or processors.*

See p. 91, refer to JVM.

As per Claim 19: Regarding: *The apparatus according to claim 14, wherein said program source code provides a virtual machine for said target processor or processors.*

See p. 91, refer to JVM.

As per Claim 20: Regarding: *The apparatus according to claim 13, wherein said program source code comprises elements of a programming language.*

~~(Program code according to claim 13, said program code comprising JAVA program elements)~~.

See Figure 1, or 3, refer to JAVA source code.

As per Claim 21: Regarding: *The apparatus according to claim 14, wherein said program source code comprises elements of a programming language.*

~~*Program code according to claim 14, said program code comprising JAVA program elements.*~~

See Figure 1, or 3, refer to JAVA source code.

As per Claim 22: Regarding: *A processor, configured in accordance with program code comprising at least one program code module of a plurality of program source code modules, for translating between high level code and instructions for a target processor, said at least one program source code module being in accordance with a characteristic of said target processor and selected from said plurality of program source code modules.*

See a computer that installed with a JVM, sec. 2.2, p. 91

As per Claim 23: Regarding: *A processor, configured by program code comprising an agglomeration of two or more program source code modules of said plurality of said program source code modules.*

See a computer that installed with a JVM, sec. 2.2, p. 91

As per Claim 24: Regarding: *A system comprising a first and second processor, said first and second processor configured in accordance with program code comprising at least two program source code modules, wherein the first of said at least two program source code modules is arranged to translate high level code to instructions for said first processor and a second of said at least two program source code modules is arranged to translate high level code to instructions for said second processor.*

See client/server computers that run with a JVM, sec. 2.2, p. 91

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
March 12, 2010

/Ted T. Vo/
Primary Examiner, Art Unit 2191